User name: SHAW (11) Queue: UIDESK/UNIX_UIMKGT
File name: Server: CLFPCD010
Directory:
Description: NORDIC40.
December 21, 1998 5:46pm

EXHIBIT
RX-577 C

```
 SSS  H   H   A   W   W
S   S H   H  A A  W   W
S     H   H A   A W W  W
 SSS  HHHHH A   A W W W
    S H   H AAAAA W W W
S   S H   H A   A WW WW
 SSS  H   H A   A W   W
```

```
L      SSS  TTTTT
L     S   S   T
L     S       T    : :
L      SSS    T    : :
L         S   T
L     S   S   T    : :
LLLLL  SSS    T    : :
```

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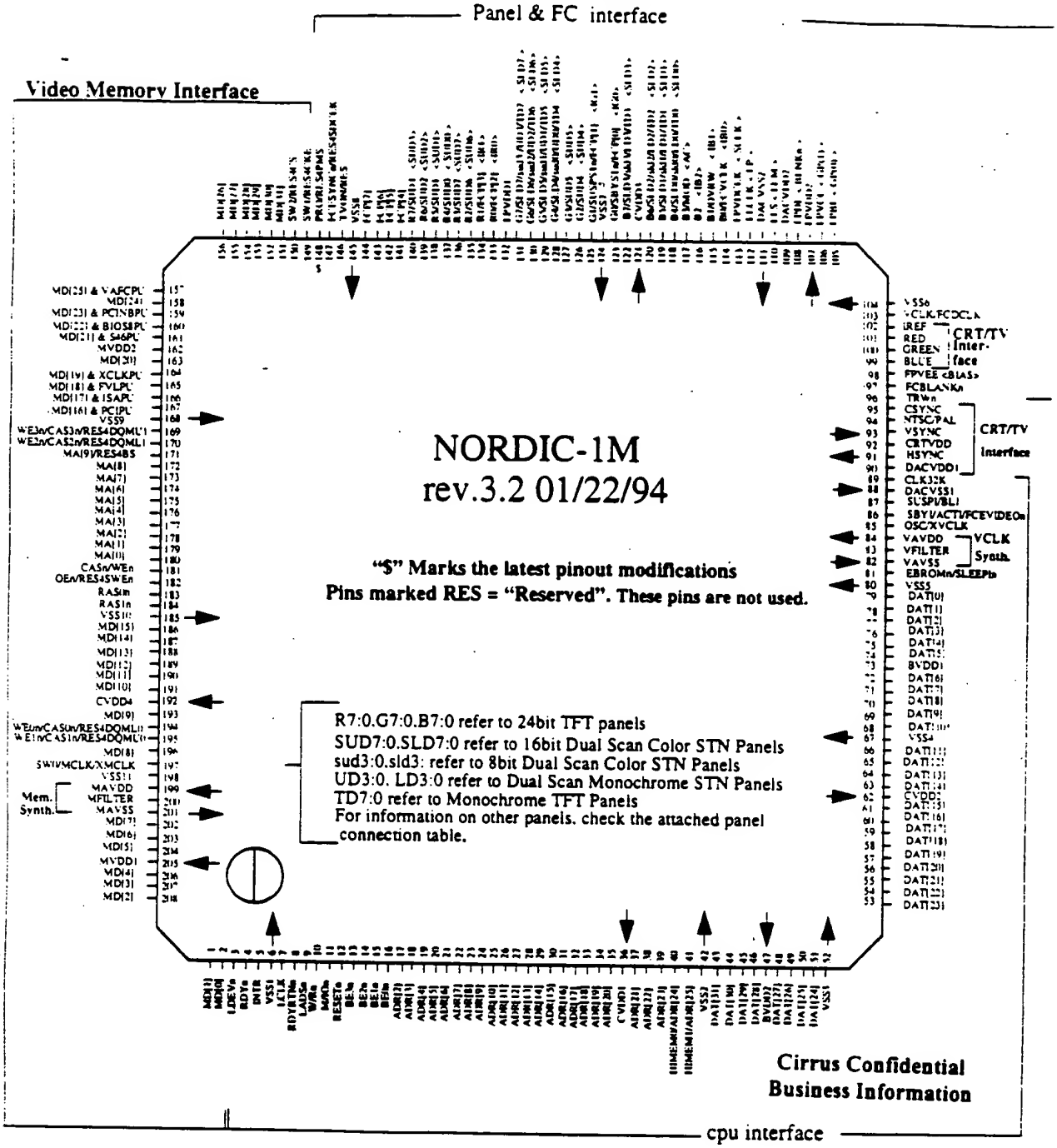
Panel & FC interface
Video Memory Interface
NORDIC-1M
rev.3.2 01/22/94
"$" Marks the latest pinout modifications
Pins marked RES = "Reserved". These pins are not used.
R7:0.G7:0.B7:0 refer to 24bit TFT panels
SUD7:0.SLD7:0 refer to 16bit Dual Scan Color STN Panels
sud3:0.sld3: refer to 8bit Dual Scan Color STN Panels
UD3:0. LD3:0 refer to Dual Scan Monochrome STN Panels
TD7:0 refer to Monochrome TFT Panels
For information on other panels. check the attached panel connection table.
CRT/TV Interface
VCLK Synth.
Mem. Synth.
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cpu interface

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DELTA LIST OVER PREVIOUS PINOUT RELEASED ON :

08/26/93:

- no POUT on SW2/POUT
- XVCLK moved from SW1/VCLK/XVCLK to OSC/XVCLK. This way SW1/VCLK/XVCLK became SW1/VCLK.

09/06/93

- All panel pins whose names were not starting with the color panel name were changed such that the names start now with the color panel pin (R7, G7, B7 and so on). So it was only a pin name change.

09/12/93 rev. 1.0 and 1.1

1. Took-out Whisper Support Pins: WWRn, WRdn, WAD[3:0], FPCn.

2. Reduced the number of CPU Address Pins: ADR[24:27] went-away. Use HIMEM to place the chip outside 16MB of memory for linear addressing.

3. Killed CRTVDD and placed CRT Interface on Host Bus VDD.

4. Introduced VAFC pins in a unique pinout configuration in both VESA VL and PCI.
Added VAFCPU a pull-up to enable VAFC (VESA Advanced Feature Connector).
ADR[27:24] become VAFC pins. and R[7:4], G[7:6] , CLK32K, SUSPI/BLI, SBYI/ACTI get a configuration for VAFC -> total 14 pins.
SW0/VCLK will be used as VAFC DCLK, losing SW0 pin as panel type when VAFCPU is used.
In PCI bus, no ADR pin will be shared with VAFC.
ASW0PU will be added on MD pins to replace SW0 pin when VAFC is enabled by VAFCPU. SW0PU will read-back in the same register bit as SW0, so the BIOS will not feel any modification in the reporting scheme. The chip will draw more power in suspend with VAFC.

5. Moved SW2, SW1/MCLK/XMCLK, the two RESERVED pins and TRWn on MVDD to prepare for SDRAM pin compatible option in the next Nordic that supports SDRAMs. It looks that we need only 3 more memory pins to support SDRAM-s so TRWn will not be used. It was moved so it is on the right VDD bus if needed.

6. Moved CVDD3, VSS3, VCLK Synth. H/VSYNC, EROMn, SW0 per Thomas Hung's request to fit the floor plan.

09/21/93

1. Added AUXS1 on D/Cn as an option to be used with CS4231S as CS.
2. Added AUXS2 on EROMn/VADRn as an option to be used for Sound Synthesizer Chip Select.
3. Rearanged 5428 FC pins due to a previous error : R5 and R4 should not be used with FC.
   - FCP[1:0] are shared with G7 and G6.
   - SW2 and the two pins reserved for SDRAM were moved in between Video Memory pins and Panel pins and one of them is used as FCESYNCn.
   - OVRWis shared with CLK32K, FCBLANKn is shared with SUSPI and FCEVIDEn is on SBYI.
4. Renamed the External Clock PU XCLKPU instead of XMCPU.

10/11/93 rev. 1.3

1. Moved some external pull-ups.
2. Added alternate pin functions on panel pins as well as actual schematic name for engineering

10/27/93

1. Added TV-OUT (called also NTSC-OUT) pins on the panel pins

10/28/93 rev. 1.5 Modifications

1. Added TVG on EBROMn/AUXS2 and took out VADR as an option on this pin.
2. Put back FCESYNCn on RES4SDCLK as an option (deleted by mistake).

11/11/93 rev.2.0 Modifications

1. Reset became RESETn, active L to correspond with the defined reset signal for VESA VL and PCI.
2. TFT Panels Data Pins R7:R0, G7:G0, B7:B0 changed and all pins got rotated to get them ordered from right to left. Due to this change now Ri=TVRi, Gi=TVGi and Bi=TVBi.

01/06/94 rev. 3.0 Modifications

1. Update Panel Data Pins based on Robin's Table.
2. Move MOD pin on a Panel Data Pin used in 18bit TFT.
3. Move OVRW on a 24bit Panel Data Pin.
4. Removed pin configuration for TV-OUT support with digital encoders. All pins marked TV... were removed. As a result, some pins like LLCLK, LFS, FPDE, FPVDCLK have one function now.
5. Removed WavePort pins, including AUDVDD: total 7 pins freed. AUX2 and TVG muxed on EBROMn are no longer needed either.
6. Added one more CPU address pin: instead of HIMEM, Nordic has now HIMEM0 and HIMEM1, corresponding to CPU Address 24 and 25 or any other external decode of the high order CPU address bits. In the process of adding this pin, most CPU Interface pins on the right side were moved to the right by one pin.
7. Added CRTVDD supplying HSYNC, VSYNC, CSYNC, NTSC/PAL CRT and TV Interfaces output buffers.
8. EBROMn is shared with TVON, the power-on signal for AD720. So, in ISA bus with on chip BIOS support, AD720 power on cannot be directly controlled by Nordic.
9. Added pins for Analog TV Encoder support - AD720 and MC1377 :
   a. CSYNC = Composite Sync signal
   b. NTSC/PAL = 1 -> NTSC, 0-> PAL (for AD720, but it is TV Encoder Dependent)
   c. EBROMn/TVON (see #8).
10. ASW0PU "Alternate Switch 0 Pull-Up" pull-up on pin 155. MD[26] was removed, as SW0 is now not multiplexed.
11. De-multiplexed some of the pins previously multiplexed:
    a. Pin 168 TWRn/RES4PMS is now RES4PMS, a pin reserved for synchronous DRAM support.
    b. SUSPI/BLI/FCBLANKn is now SUSPI/BLI, not affected by the Feature Connector Enable Configuration
    c. As a consequence of b, pin 97 is FCBLANKn (not muxed with anything). Please note that FCEVIDEOn is still muxed with SBYI/ACTI as before, as Standby Input and Keyboard Activity are less important functions in a system.
    d. SW0 is no longer muxed on VCLK/FCDCLK. So VLK/FCDCLK is a pin but it moved to pin 103 in the PVDD area, to be consistent with FC power supply.
12. SW1, muxed on MCLK/XMCLK (pin197) became SW0. This is just a name change to have the switches placed in a more consistent manner.

CL 152803

13. SW1 is now muxed with a reserved pin: RES4CKE, pin 148, which before was totally reserved. The idea here is to go for pu/pd with SDRAM-s for SW2 and SW1, while keeping SW0 on MCLK even with SDRAM-s.
14. Pin 147 is Reserved. It is actually one of the WavePort pins, but placed in-between Memory and Panel VDD busses (on MVDD) for maximum flexibility. To acheive this, the pins on its right were moved to the right by one FPVEE <BIAS> moved down to pin 98 (it was 105).
15. TRWn is now by itself on pin 96, on FPVDD.
16. The names of all flat panel data pins reflect the panel type table attached to this document.

01/13/94 rev. 3.1 Modifications

1. On EBROMn/TVON -> EBROMn/SLEEPIn with SLEEPIn an input which if L puts Nordic to sleep (as 3C3[0] and 46E8(3).
2. TVON is now on RES, but TVON/RES is pin 146 and FCESYNCn/RES4SDCLK is pin 147.

01/22/94 rev. 3.2 Modifications

1. Pin 148, RES4PMS which was a pin resurved for synchronous DRAM-s, got a function: it is now a programable output PRO and it is on FPVDD instead of MVDD. The intention is to optionally use this pin to control a switch between 5V and 3.3V, in which case a H level of 5V is desirable. My primary choice for this function is actually NTSC/PAL pin which is on CRTVDD, but if the TV-OUT option is used in a system and a switch between 5 and 3.3V is provided, PRO may be used.

CL 152804

Panel Interface Data Formats (compatible with 62xx family except 18/24 bit TFT)

TFT 24/ 18/ 12/ 9 bit Name	Pin	DB44#	STN Color 16bit/8bit	Monochrome dual STN / single TFT
R7/R5/R3/R2	141	(13)	SUD3 / ---	---
R6/R4/R2/R1	140	(14)	SUD2 / ---	---
R5/R3/R1/R0	139	(15)	SUD1 / ---	---
R4/R2/R0	138	(16)	SUD0 / ---	---
R3/R1	137	(9)	SUD7 / ---	---
R2/R0	136	(10)	SUD6 / ---	---
R1	135		---	---
R0	134		---	---
G7/G5/G3/G2	132	(8)	SLD7 / sud3	UD3 / TD7
G6/G4/G2/G1	131	(7)	SLD6 / sud2	UD2 / TD6
G5/G3/G1/G0	130	(6)	SLD5 / sud1	UD1 / TD5
G4/G2/G0	129	(5)	SLD4 / sud0	UD0 / TD4
G3/G1	128	(11)	SUD5 / ---	---
G2/G0	127	(12)	SUD4 / ---	---
G1	126		---	---
G0	125		---	---
B7/B5/B3/B2	123	(4)	SLD3 / sld3	LD3 / TD3
B6/B4/B2/B1	121	(3)	SLD2 / sld2	LD2 / TD2
B5/B3/B1/B0	120	(2)	SLD1 / sld1	LD1 / TD1
B4/B2/B0	119	(1)	SLD0 / sld0	LD0 / TD0
B3/B1	118		---	---
B2/B0	117		---	---
B1	116	(23)	MOD	MOD
B0	115		---	---
FPVDCLK	114	(18)	SCLK / XCLKL	SCLK
LLCLK	113	(35)	LP	LP
LFS	111	(22)	FLM	FLM
FPDE	109	(26)	--- / XCLKU	/ DE

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